JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

III Year - II Semester		L	T	P	C
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VLSI LAB					

List of Experiments

PART (A): FPGA Level Implementation (Any Seven Experiments)
Note 1: The students need to develop Verilog /VHDLSource code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary Synthesizer.
Note 2: All the experiments need to be implemented on the latest FPGA/CPLD Hardware in the Laboratory

1. Realization of Logic gates

   Design and Implementation of the following:

2. 4-bit ripple carry and carry look ahead adder using behavioural, dataflow and structural modeling
3. a) 16:1 mux through 4:1 mux
   b) 3:8 decoder realization through 2:4 decoder
4. 8:3 encoder
5. 8-bit parity generator and checker
6. Flip-Flops
7. 8-bit synchronous up-down counter
8. 4-bit sequence detector through Mealy and Moore state machines.

EDA Tools/Hardware Required:

1. EDA Tool that supports FPGA programming including Xilinx Vivado /Altera (Intel)/ Cypress/Equivalent Industry standard tool along with corresponding FPGA hardware.
2. Desktop computer with appropriate Operating System that supports the EDA tools.

PART (B): Back-end Level Design and Implementation (Any Five Experiments)

Note: The students need to design the following experiments at schematic level using CMOS logic and verify the functionality. Further students need to draw the corresponding layout and verify the functionality including parasites. Available state of the art technology libraries can be used while simulating the designs using Industry standard EDA Tools.

Design and Implementation of the following

a. Universal Gates
b. An Inverter
2. Full Adder
3. Full Subtractor

4. Decoder
5. D-Flip-flop

EDA Tools/Hardware Required:

- Mentor Graphics Software / Cadence/Synopsys/Tanner or Equivalent Industry Standard/CAD Tool.
- Desktop computer with appropriate Operating System that supports the EDA tools.